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BMS Institute of Technology and Management

(An Autonomous Institution Affiliated to VTU, Belagavi)
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Department of Electronics and Communication Engineering

M.Tech.-VLSI System Design (VSD)

Report on One-Day Physical Design Hackathon - RTL-to-GDSII ASIC Design Hackathon

Date: 31.07.2026

Event Details

Title: RTL-to-GDSII Physical Design Hackathon using Industry Standard EDA Tools

Evaluator:

Mr. Bhaskar G. R.

Physical Design Engineer,
Wipro VLSI, Bengaluru

Participants:

M.Tech. II Semester – VLSI System Design Students

Venue:

M.Tech. VLSI Laboratory,
Department of ECE,
BMS Institute of Technology and Management

The Department of Electronics and Communication Engineering organized a **One-Day Physical Design Hackathon** for the II Semester M.Tech. (VLSI System Design) students as part of the **Physical Design IPCC Laboratory and SystemVerilog Continuous Comprehensive Assessment (CCA)**. The Hackathon was conducted to evaluate the students through a complete industrial ASIC design flow instead of the conventional laboratory examination pattern. The activity enabled students to integrate the knowledge gained from RTL design, SystemVerilog verification, synthesis, and physical design using industry-standard EDA tools.

The Hackathon was evaluated by **Mr. Bhaskar G. R., Physical Design Engineer, Wipro VLSI, Bengaluru**, who has more than fourteen years of experience in ASIC Physical Design and semiconductor product development. The event provided students with valuable exposure to industrial design methodologies, implementation practices, and technical discussions followed in semiconductor companies.

Objectives of the Hackathon

The major objectives of the Hackathon were:

- To design synthesizable RTL using SystemVerilog.

- To perform functional verification using SystemVerilog testbench architecture.
- To achieve functional coverage and verify complete design correctness.
- To synthesize RTL into technology-mapped gate-level netlists.
- To perform complete ASIC physical implementation from RTL to GDSII.
- To analyse timing, area, congestion and power reports.
- To demonstrate industrial ASIC implementation methodology.
- To improve debugging, optimization and problem-solving skills.

Hackathon Design Problems

Each student selected one digital design problem and completed the entire RTL-to-GDSII implementation flow.

The design problems included:

1. 8-Tap FIR Filter
2. SDRAM Controller
3. Memory Built-In Self-Test (MBIST)
4. Two-Way Set Associative Cache Controller
5. 16×16 Pipelined Wallace Tree Multiplier
6. Router 1×3 – Packet Switching Fabric for NoC
7. 4×4 Matrix Multiplier with Integrated SRAM
8. UART Controller (RTL-to-GDSII)
9. AHB-to-APB Bridge
10. AXI4-Lite to AXI4-Stream Bridge
11. FSM-Based Master–Slave Communication System, etc.

Hackathon Workflow

Each team completed the complete ASIC implementation flow consisting of:

- Problem understanding and architecture development
- RTL design using SystemVerilog
- Functional simulation
- Driver, Monitor, Scoreboard and Functional Coverage implementation
- Logic synthesis
- Timing analysis
- Floorplanning
- Power planning
- Standard cell placement
- Clock Tree Synthesis (CTS)
- Routing
- Physical verification
- Timing optimization
- Report generation
- Final design presentation

EDA Tools Used

The Hackathon utilized industry-standard EDA tools including:

- Vivado

- Cadence Genus
- Cadence Innovus
- Synopsys Design Compiler

Evaluation Methodology

Students were evaluated continuously based on:

- RTL quality
- Functional correctness
- Verification methodology
- Functional coverage
- Synthesis reports
- Timing closure
- Physical implementation quality
- Area optimization
- Power optimization
- Final technical presentation
- Technical viva conducted by the industry expert

Key Technical Learning Outcomes

During the Hackathon, students learned:

- Complete RTL-to-GDSII ASIC implementation methodology.
- SystemVerilog verification flow.
- Functional coverage driven verification.
- Importance of synthesis constraints.
- Floorplanning strategies.
- Power planning methodologies.
- Placement optimization.
- Clock Tree Synthesis techniques.
- Routing congestion analysis.
- Static Timing Analysis.
- Design Rule Check (DRC).
- Area and power optimization.
- Debugging of synthesis and physical implementation issues.

Industry Expert Interaction

Mr. Bhaskar G. R. interacted with every student team and evaluated:

- RTL coding practices
- Verification methodology
- Functional coverage implementation
- Synthesis optimization
- Floorplanning strategy
- CTS implementation
- Routing quality
- Timing reports
- Slack analysis
- Area optimization

- Power optimization
- Physical verification reports
- Final implementation methodology

The expert also discussed about job market, preparation strategies, and several real industrial case studies related to timing closure, congestion optimization, design constraints, and backend implementation followed etc.

Outcome of the Hackathon

The Hackathon successfully bridged the gap between academic laboratory practice and industrial ASIC implementation. Students gained hands-on experience in complete RTL-to-GDSII design flow and developed confidence in using industry-standard EDA tools. The event enhanced their skills in digital design, functional verification, synthesis, physical design, timing analysis, , and technical presentation. The Hackathon also strengthened students' readiness for careers in RTL Design, Verification, Physical Design, Static Timing Analysis, Design for Testability, and ASIC implementation.




PG-VSD Coordinator
Dr. Banuprakash R


HoD ECE
Dr. A Shobha Rani